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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/648,390	08/27/2003	Isao Nojiri	57454-965	5313

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EXAMINER	
NGUYEN, DANNY	

ART UNIT	PAPER NUMBER
2836	

DATE MAILED: 03/11/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/648,390	NOJIRI ET AL.	
	Examiner	Art Unit	
	Danny Nguyen	2836	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 December 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-5* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,4,5* is/are rejected.

7)☒ Claim(s) *3* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments filed 12/02/2004 with respect to claims 1, 2, 4, and 5 have been fully considered but they are not persuasive.

Regarding claims 1, 2, 4, applicant argued that Ker does not disclose that the ESD protection protects the internal circuit from ESD event, which is generated at the first input terminal, and the first input terminal receives an external voltage. The arguments are not convincing. Ker provides the ESD protection circuit protects the ESD event, which is generated at the first input terminal (803) (e.g. col. 4, lines 58-65). The input pad (803) is considered as the input voltage terminal. It normally gets a voltage applied to it. If the voltage become too large applied to the input pad, which is positive with respect to Vss, it conducts diodes (809) and if the voltage gets too large applied to the input pad, which is negative with respect to Vdd, it conducts diodes (808) (col. 5, lines 6-22). The applicant's arguments do not distinguish over the Ker reference.

In response to applicant's argument with respect to claim 5 that there is no suggestion to combine the references, the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988)and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, Narita discloses the ESD protection circuit (such as 11) is a single diode, which is

connected between power, supply Vdd and the common line 10. Narita only lacks the ESD protection comprises a plurality of diodes. However, providing the ESD protection circuit which comprises a plurality of diodes is well known the art and disclosed by Ker. Ker discloses an example of the ESD protection circuit comprises a plurality of diodes, which are connected between the power supply and common line (see fig. 8) provides a better ESD protection (col. 1, lines 44-60).

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

2. Claims 1, 2, 4 are rejected under 35 U.S.C. 102(a) as being anticipated by Ker et al (USPN 6,649,944).

Regarding claim 1, Ker discloses a semiconductor device (fig. 8) comprises a first input terminal (803) receiving a first positive voltage (it normally gets a voltage applied to it that is positive with respect to the Vss line) externally in an inspection of said semiconductor device and a normal operation of the semiconductor device; an internal circuit (810) connected to the first input terminal and performing a prescribed operation; and a first protection circuit (809) protecting the internal circuit from static electricity generated at the first input terminal, the first protection circuit including a plurality of first diode elements (such as Dd1 to Ddn) connected in series between the first input terminal and a line of a reference potential

(Vss) and conducting in response to a voltage of the input terminal exceeding a second positive voltage higher than the first positive voltage (e.g. col. 4, lines 27-58), and a second diode element (802) connected between the line of the reference potential and the first input terminal.

Regarding claim 2, Ker discloses a second input terminal (803) connected to the internal circuit (810) and receiving a first negative voltage (the input pad is considered as a second input terminal receives a voltage applied to it which is negative with respect to Vdd); and a second protection circuit (803 and 808) protecting the internal circuit from static electricity generated at the second input terminal; wherein the second protection circuit includes a plurality of third diode elements (Du1 to Dun) connected in series between the line of the reference potential (Vss) and the second input terminal (805) and conducting in response to a voltage of the second input terminal going lower than a second negative voltage lower than the first negative voltage, and a fourth diode element (803) connected between the second input terminal and the line of the reference potential (col. 4 and 5, lines 66-21).

Regarding claim 4, Ker discloses a semiconductor device (fig. 8) comprises an input terminal (803) receiving a first negative voltage externally in an inspection of the semiconductor device and a normal operation of the semiconductor device; an internal circuit (810) connected to the input terminal and performing a prescribed operation; and a protection circuit (804 and 809) protecting the internal circuit from static electricity generated at the input terminal, the protection circuit including a plurality of first diode elements (Dd1 to Ddn) connected in series between a

line of a reference potential and the input terminal and conducting in response to a voltage of the input terminal going lower than a second negative voltage lower than the first negative voltage, and a second diode element (804) connected between said input terminal and the line of said reference potential (col. 4 and 5, lines 66-21).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Narita (USPN 5953191) in view of Ker. Narita discloses a semiconductor device (e.g. fig. 1) comprises an input terminal receiving externally a voltage (Vdd) of at most a first positive voltage and at least a first negative voltage (Vss) in an inspection of the semiconductor device and a normal operation of the semiconductor device; an internal circuit (1) connected to the input terminal and performing a prescribed operation; and a protection circuit protecting (such 11) the internal circuit from static electricity generated at the input terminal. Narita does not disclose the protection circuit as claimed. Ker discloses a protection circuit (fig. 8) comprises a plurality of first diode elements (e.g. Du1 to Dun) connected in series between a input terminal and a line of a reference potential and conducting in response to a voltage of the input terminal exceeding a second positive voltage higher than the positive voltage (e.g. col. 4, lines 27-58), and a plurality of second diode elements (Dd1 to Ddn) connected in series between the line of

the reference potential and the input terminal and conducting in response to the voltage of said input terminal going lower than a second negative voltage lower than the first negative voltage (col. 4 and 5, lines 66-21). It would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the circuit of Narita to incorporate the protection circuit including a plurality of diodes as disclosed by Ker in order to provide a better ESD protection (col. 1, lines 44-60).

Allowable Subject Matter

4. Claim 3 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Danny Nguyen whose telephone number is (571)-272-2054. The examiner can normally be reached on Mon to Fri 8:00 AM to 4:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Brian Sircus can be reached on (571)-272-2058. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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2/25/2005

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